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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/723,432	11/25/2003	Astrid Elbe	S0193.0008	6238

38881 7590 12/07/2007

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EXAMINER	
RAHMAN, FAHMIDA	
ART UNIT	PAPER NUMBER
2116	

MAIL DATE	DELIVERY MODE
12/07/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/723,432	ELBE ET AL.	
	Examiner	Art Unit	
	Fahmida Rahman	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 September 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-14,16 and 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-14 and 18* is/are rejected.

7)☐ Claim(s) *16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *8/16/06* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This final action is in response to communications filed on 9/7/2007.

2. Claims 1, 15, 17 have been cancelled, claims 2-5, 7-11, 13-14, 16 and 18 have been amended, no new claims have been added. Thus, claims 2-14, 16 and 18 are pending.

Claim Objections

Claims 3, 16, 18 are objected to because of the following informalities:

"a common chip" recited in claim 3 should be "the common chip" as it is recited earlier in claim 18.

"An electronic circuit" in line 1 of claim 16 should be changed to "The electronic circuit" as claim 18 recites the limitation.

"said oscillator" in line 12 of claim 18 lacks antecedent basis.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al (US Patent 5708801), in view of Alasti et al (US Patent 6263390).

For claim 2, Williams et al teach the following limitations: **The electronic circuit comprising: a processing unit** (13) **having a clock connection for receiving a first clock** (CHIP CLOCK) **and a data connection** (13 receives data from 14, therefore 13 has a data connection); **a peripheral unit** (14) **having a clock connection and a data connection** (Fig 1); **synchronization means comprising a first and a second data connection** (16 takes data from 11 and pass it to 13), **said first data connection being connected to said data connection of said peripheral unit** (the output of 16 is connected to 14 via 13); **and a data bus being connected to said data connection of said processing unit and to said second data connection of said synchronization means** (16 and 13 are connected to each other through two connections. Thus, it comprises a bus), **wherein said processing unit** (13), **said peripheral unit** (14), **said synchronization means** (16) **and said data bus** (bus between 13 and 16) **are arranged on a common chip** (15 is a chip) **having two external connection devices being arranged to be connectable to two corresponding contact connections of a terminal** (bus 11 and clock generator 12 are connected to the chip), **a first of said external connection devices being connected to said clock connection of said peripheral unit** (11 is connected to the peripheral unit 14 and provide bus clock to 14) **and the second of said external**

connection devices being connected to said clock connection of said processing unit (12 is connected to 13 and provide CHIP clock to 13) **so that the peripheral unit receives a second clock which is different from the first clock** (CHIP clock and bus clock are different as explained in lines 50-60 of column 2).

Williams does not teach the following limitations: the first clock and the second clock is independent

Alasti et al teach the following limitations:
CPU receives a first clock (CPU clock of Fig 1);
peripheral unit (104, 106, 108 in Fig 1) **receives a second clock which is independent from the first clock** (lines 47-51 of column 3)

It would have been obvious for an ordinary skill in the art at the time the invention was made to combine the teachings of Williams and Alasti. One ordinary skill would be motivated to combine the teachings of Williams and Alasti, as an independence provides the flexibility of operation between two units. One ordinary skill would be further motivated to include the chip in a card, since placing chip in a card is necessary in designing many systems.

The combined teachings of Williams, Alasti do not teach the chip card. Examiner takes an official notice that chip laid on a chip card is well known in the art. One ordinary skill

would be motivated to include the electronic circuit in a chip card, since chip card including electronic circuit is widely used in credit card, or cash card.

4. Claim 3, 4, 5, 6, 7, 9, 13, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamada et al (US patent 5017766), in view of Reichmeyer et al (US Patent 5973617).

For claim 13, Tamada et al teach the following limitations:

A method of controlling an electronic circuit (Fig 2) having a central processing unit (27) and a peripheral unit (32) being connected to each other via a data bus (38), wherein said central processing unit and said peripheral unit are arranged on a common chip card (lines 30-35 of column 2), comprising:

- clocking said central processing unit by a first clock (output of 25 in Fig 2) using an external connection device ("terminal equipment" mentioned in line 50 of column 3) of the common chip card, being arranged to be connectable to a corresponding contact connection of a terminal (contact section 3 in Fig 2, lines 48-52 of column 3);

- clocking said peripheral unit by a second clock (lines 25-30 of column 4) using a oscillator of the electronic circuit (33 in Fig 2; lines 25-30 of column 4), the oscillator being independent from the first clock (the oscillator connected to 32 is independent of clock output from 25)

- and synchronizing data transmitted between said central processing unit and said peripheral unit via said data bus (year-month-date data is generated by peripheral as mentioned in line 30 of column 4, which is displayed as 4 in Fig 1 through CPU as mentioned in line 41 of column 4. As CPU send the data, data is synchronized to CPU's clock).

Tamada et al do not teach the following limitations: The oscillator is a controllable oscillator.

Reichmeyer et al teach a system where a controllable oscillator (SBOSC in Fig 1; lines 5-7 of column 5) controls a timer (Fig 1).

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Tamada et al and Reichmeyer et al, since controllable oscillator provides flexible operation.

For claim 18, Tamada et al mention the following limitations:

An electronic circuit comprising:

- a central processing unit (27) havinq a clock connection for receiving a first clock (output of 25) and a data connection (connection with 38);
- a peripheral unit (32) having a clock connection (321) and a data connection (323);
- synchronization means (21) comprising a first (I/O data) and a second data connection (connection to 38), said first data connection being connected to said data connection of said peripheral unit (Fig 2); and

- a data bus (38) beinq connected to said data connection of said central processing unit (Fig 2) and to said second data connection of said synchronization means (Fig 2),
- wherein said central processing unit, said peripheral unit, said synchronization means, said data bus and oscillator (33, lines 25-30 of column 4) are arranged on a common chip card (lines 32-35 of column 2), said clock connection of said peripheral unit is connected to said signal output of said oscillator (lines 25-30 of column 4), said clock connection of said central processing unit is coupled to an external connection device ("terminal equipment" mentioned in lines 1-6 of column 4) being arranged to be connectable to a corresponding contact connection of a terminal (3), and said oscillator being independent from the first clock (CPU clock does not control the 32.768 KHz oscillator).

Tamada et al do not teach the following limitations: The oscillator is a controllable oscillator.

Reichmeyer et al teach a system where a controllable oscillator (SBOSC in Fig 1; lines 5-7 of column 5) controls a timer (Fig 1).

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Tamada et al and Reichmeyer et al, since controllable oscillator provides flexible operation.

For claims 3, 4, 9, the IC card is an embedded cryptographic controller (lines 35-40 of column 3 of Tamada et al) with CPU, peripheral unit, synchronization means, data bus, oscillator.

For claim 5, Reichmeyer et al teach controlling means to control oscillator (SBOSC in Fig 1; lines 5-7 of column 5).

For claim 6, lines 39-42 of column 3 of Reichmeyer et al mention that standby oscillator is adjusted during wake-up periods (i.e., depending on energy available). During wake-up period main controller and main oscillator are turned on (lines 10-16 of column 7) and therefore, the energy is distributed to peripheral unit and processing unit.

For claim 7, SBCLK in Reichmeyer et al is on during wake up period while MOSC is turned off. Thus, the oscillator SBOSC is controllable to provide wake up signal when microcontroller is turned off. Thus, the frequency of output of controllable oscillator is faster than CPU clock during standby operation.

5. Claims 8, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamada et al (US patent 5017766), in view of Reichmeyer et al (US Patent 5973617), further in view of Alasti et al (US Patent 6263390).

For claims 8 and 14, Tamada et al and Reichmeyer et al do not explicitly mention about having common divisor. However, such designs are within the scope of the invention. Properly chosen frequencies of Alasti do not have common divisor (lines 25-30 of column 7 mention that PCI clock ranges from 0 to 66 Mhz, CPU clock ranges from 250 to 300 Mhz. Therefore, suitable choice of PCI and CPU frequencies provides prime relationship, such as CPU clock 200 Mhz and PCI clock 43111 Hz).

It would have been obvious for an ordinary skill in the art at the time the invention was made to provide an output signal which has no common divisor with CPU clock as taught in Alasti, since this provides a better control of peripheral unit

6. Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamada et al (US patent 5017766), in view of Reichmeyer et al (US Patent 5973617), in view of Applicant's Admission of Prior Art.

For claim 10, AAPA shows 920a and 920b as coprocessors. Since, Fig 6 is a cryptography controller, it must process some cryptographic algorithm.

For claim 11, Fig 6 of AAPA comprises two coprocessors. However, AAPA does not mention that the peripheral unit being connected to oscillator.

Examiner takes an official notice that coprocessor connected to controllable oscillator is well known in the art. One ordinary skill in the art would have been motivated to connect controllable oscillator to coprocessor, since controllable oscillator produce clock to operate the coprocessors.

For claim 12, the two coprocessors operate in parallel performing various tasks as mentioned in [0012] of AAPA. Since Fig 6 shows the cryptography controller, the tasks should be encrypting/decrypting.

Allowable Subject Matter

Claim 16 would be allowable if rewritten to include all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments with respect to claim 2-14, 16 and 18 have been considered but are moot in view of the new ground(s) of rejection. As Alasti is still relied upon for rejection, Examiner is addressing arguments regarding Alasti.

Applicant argues that Williams and Alasti fails to disclose the two independent clock signals. Examiner disagrees as lines 48-51 of column 3 of Alasti mention about clock rate independence of communications over connection 110 and over connections 112, 114, 116.

Official notice not argued by the applicant is taken as admitted prior art.

Claim 18 was indicated allowable with the condition of incorporating limitations of base claim. As the claim does not contain many limitations of base claim, the allowability is withdrawn.

Conclusion

The following is an examiner's statement of reasons for allowance: Claim 16 now depends on claim 18, which requires controllable oscillator being controlled independent from the CPU clock. Yamamoto was relied upon for rejecting claim 16. As Yamamoto is able to take multiple clock signals as inputs (columns 17-26 of column 9 mention that clock signals are fed from external pins 121), the clock frequencies can be made independent. However, Yamamoto's oscillator mentioned in line 24 of column 9 are connected to external pins 121 and controlled by clock inputs, including the CPU clock, which is not consistent with the limitation "controllable oscillator being controlled independent from the first clock."

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fahmida Rahman whose telephone number is 571-272-8159. The examiner can normally be reached on Monday through Friday 8:30 - 5:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Fahmida Rahman
Examiner
Art Unit 2116

A. ELAMIN
PRIMARY EXAMINER